EPI Forum

Paris, 6-7 October, 2025

European Processor Initiative

EUROHPC PERSPECTIVE

Alexandra Kourfali

EuroHPC
Joint Undertaking

EuroHPC Flagships: RISC-V and ARM for Energy-Efficient, Sovereign Supercomputers

EPI Forum

7th October 2025 | **Dr. Alexandra Kourfali** | Paris, FR

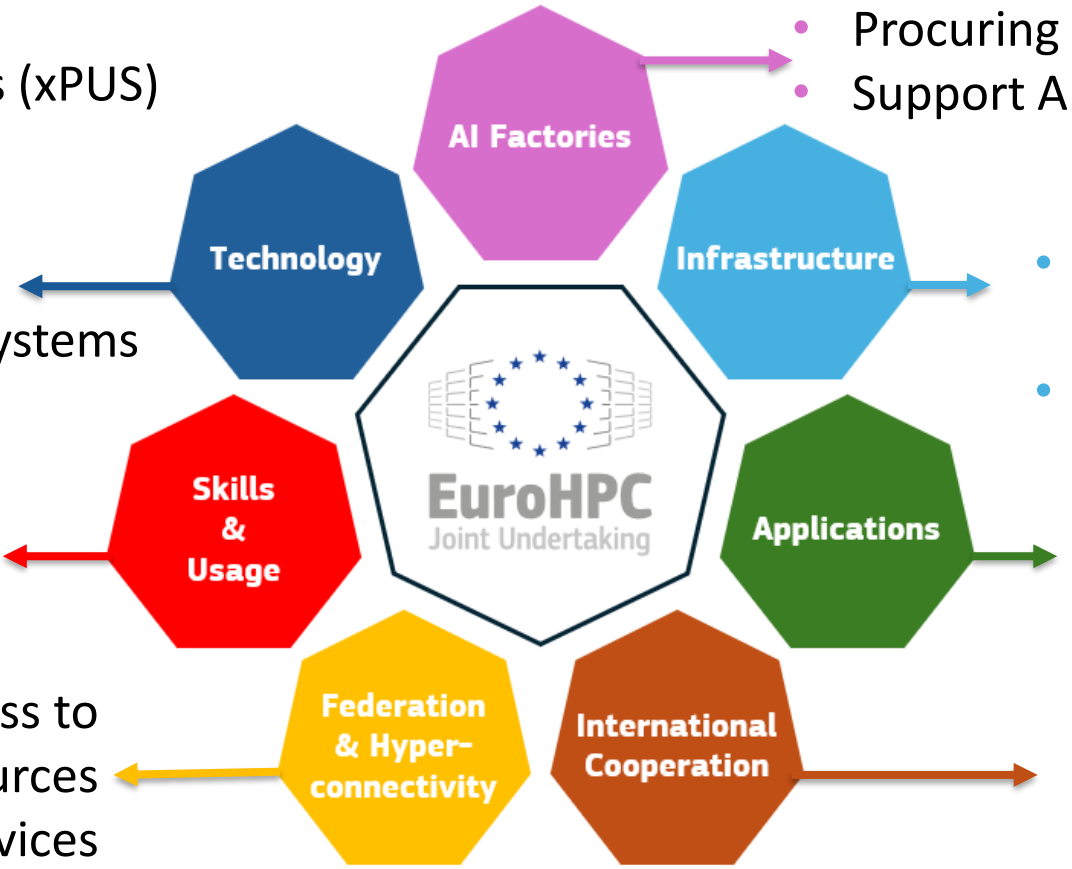
EuroHPC JU

R&I activities to develop:

- **Hardware** components (xPUS)
- **Pilots**
- **Software** stack
- **Quantum** integration
- **Energy-efficient** HPC systems

- **Training** programmes to develop HPC skills base in Europe

- Development of access to **federated** HPC resources and services



- Procuring /upgrading **AI**-oriented **HPC systems**
- Support AI app development in EU

- **Procuring**/deploying HPC & QC SOTA systems
- Providing **access** to EU users

- Algorithms, SW development
- **Centers of Excellence**

Collaboration with **3rd countries**

- Solve global challenges
- Strengthen EU competitiveness

EuroHPC infrastructure: update

HPC Systems

1 EXASCALE

- JUPITER, #1 GREEN500

3 PRE-EXASCALE

- Lumi, FI #5 TOP500
- Leonardo, IT #7
- Marenostrum 5, ES #8

5 PETASCALE

- Vega, SL
- Karolina, CZ
- Discoverer, BG
- Meluxina, LU
- Deucalion, PT

Ongoing

EXASCALE: Alice Recoque, FR

Quantum

- **8 quantum computers**
- **2 quantum simulators**

Consortia of 30+ countries

AI Factories

EuroHPC supercomputers

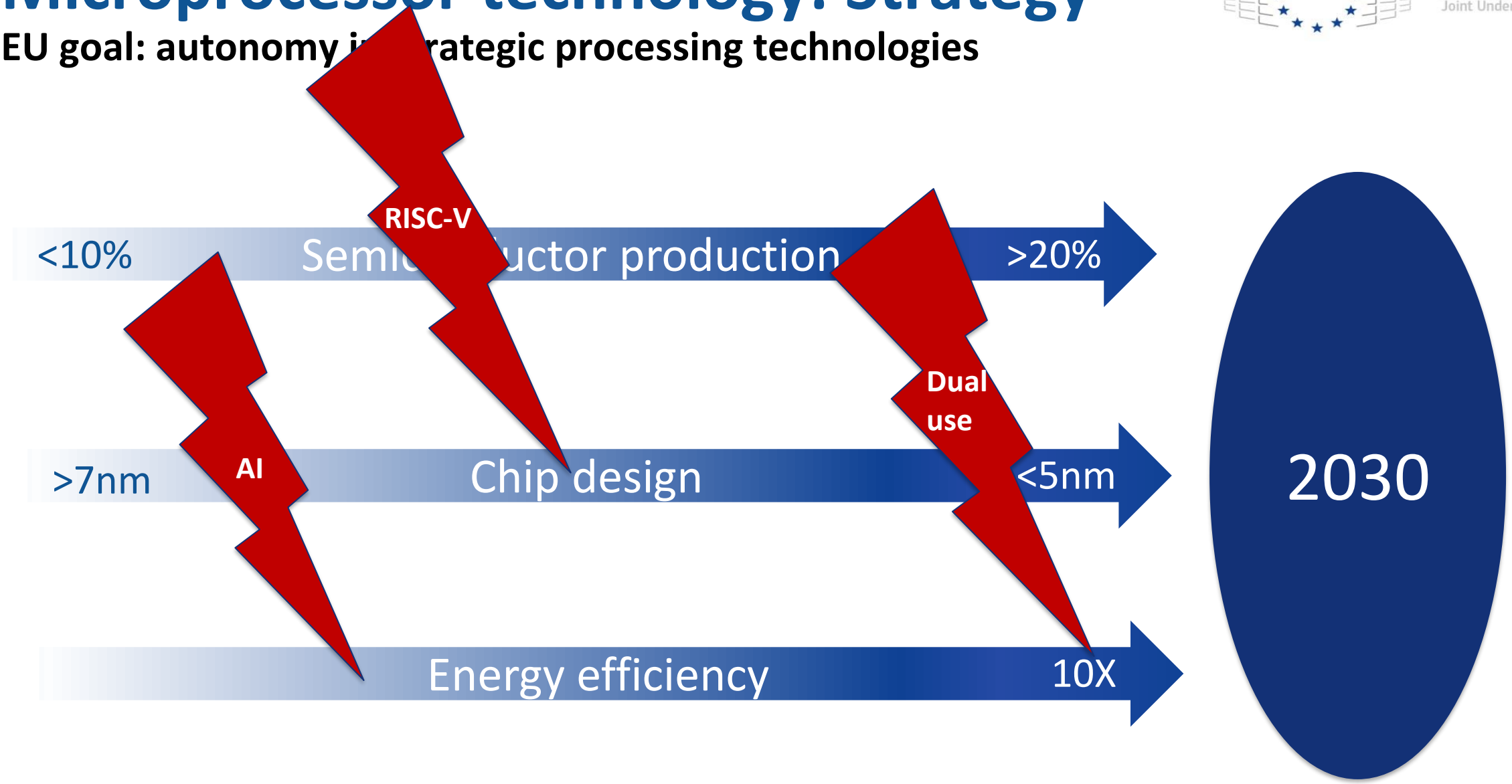
- AI-ready
- AI-upgrades
- AI-optimized

Consortia of 21+ countries

13 EU sites selected

Microprocessor technology: Strategy

EU goal: autonomy in strategic processing technologies



HPC microprocessor technology: Strategy

EU goal: autonomy in strategic processing technologies

DESIGN

Short term (2025-27)

Medium term (2028-30)

Long term (2030-)

First IPs

- **Build on EPI** efforts
- From test chips to **TRL 9**
- RISC-V processors and accelerators: chiplets, advanced nodes
- EuroHPC exascale systems as first customer

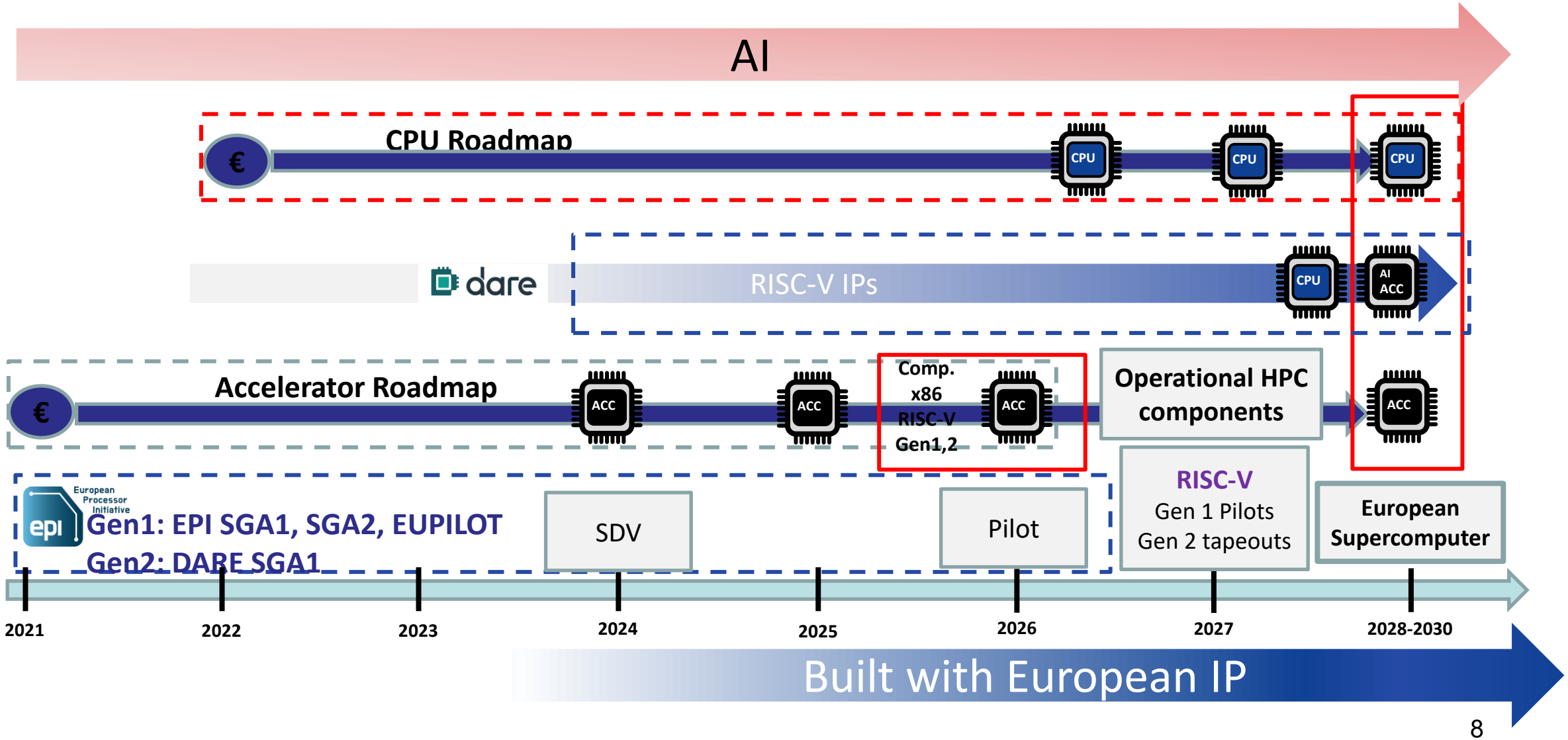
New RISC-V architectures complement the work of EPI and DARE

- Pilots on RISC-V with stand-alone competitive xPUs
- Collective effort building on **EU R&D** in low power, AI, security,…,
- EuroHPC **post-exascale** system as first customer

Post-exascale RISC-V systems based on EU R&D

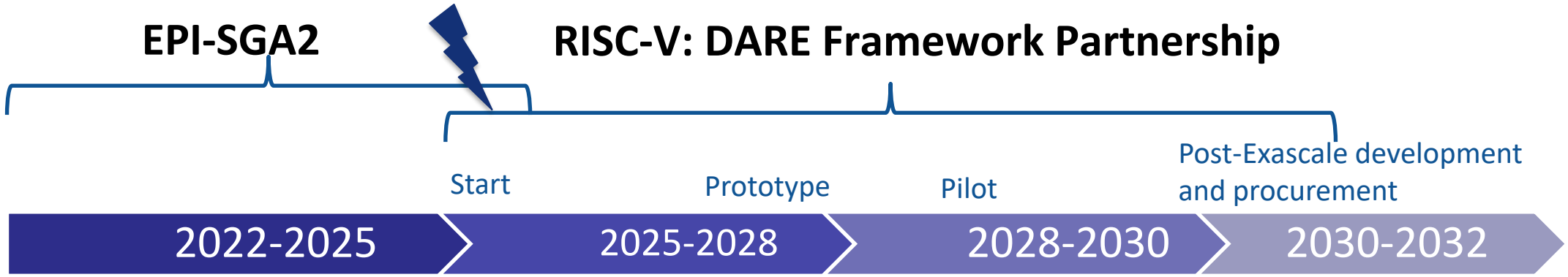
- **RISC-V ISA plays a central role on EU's technology strategy**
- ***AI, quantum, and sovereign needs are reforming EU's strategy in processors***

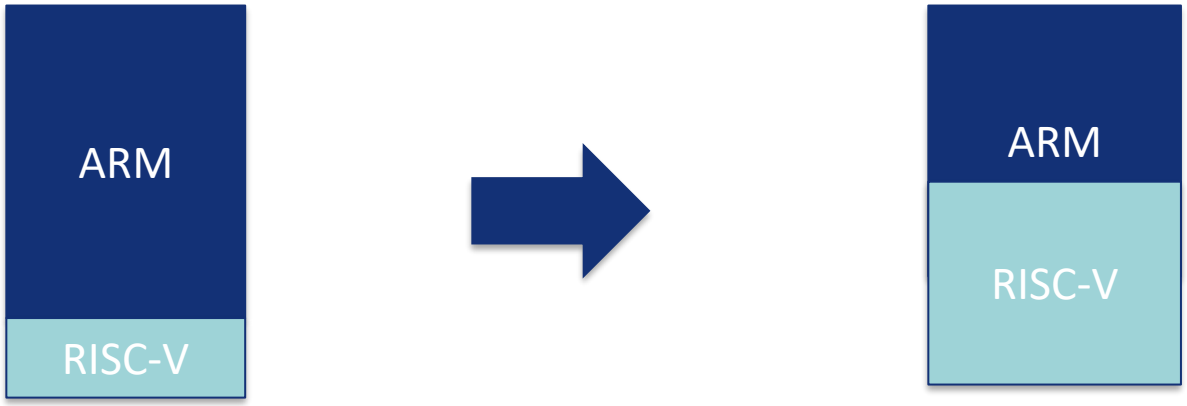
EuroHPC Chips Flagships Roadmap



EuroHPC flagships

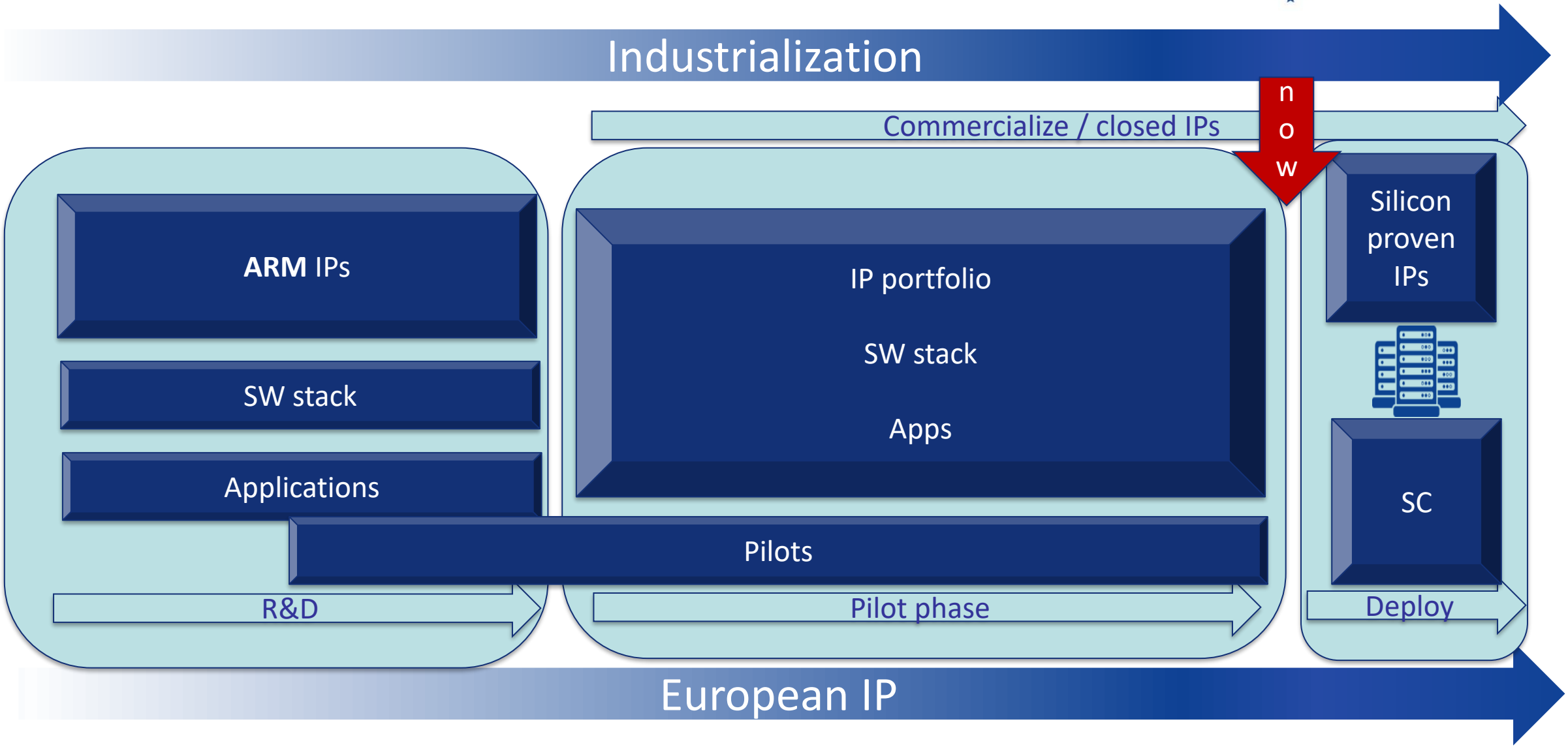
Microprocessor technology: State of play



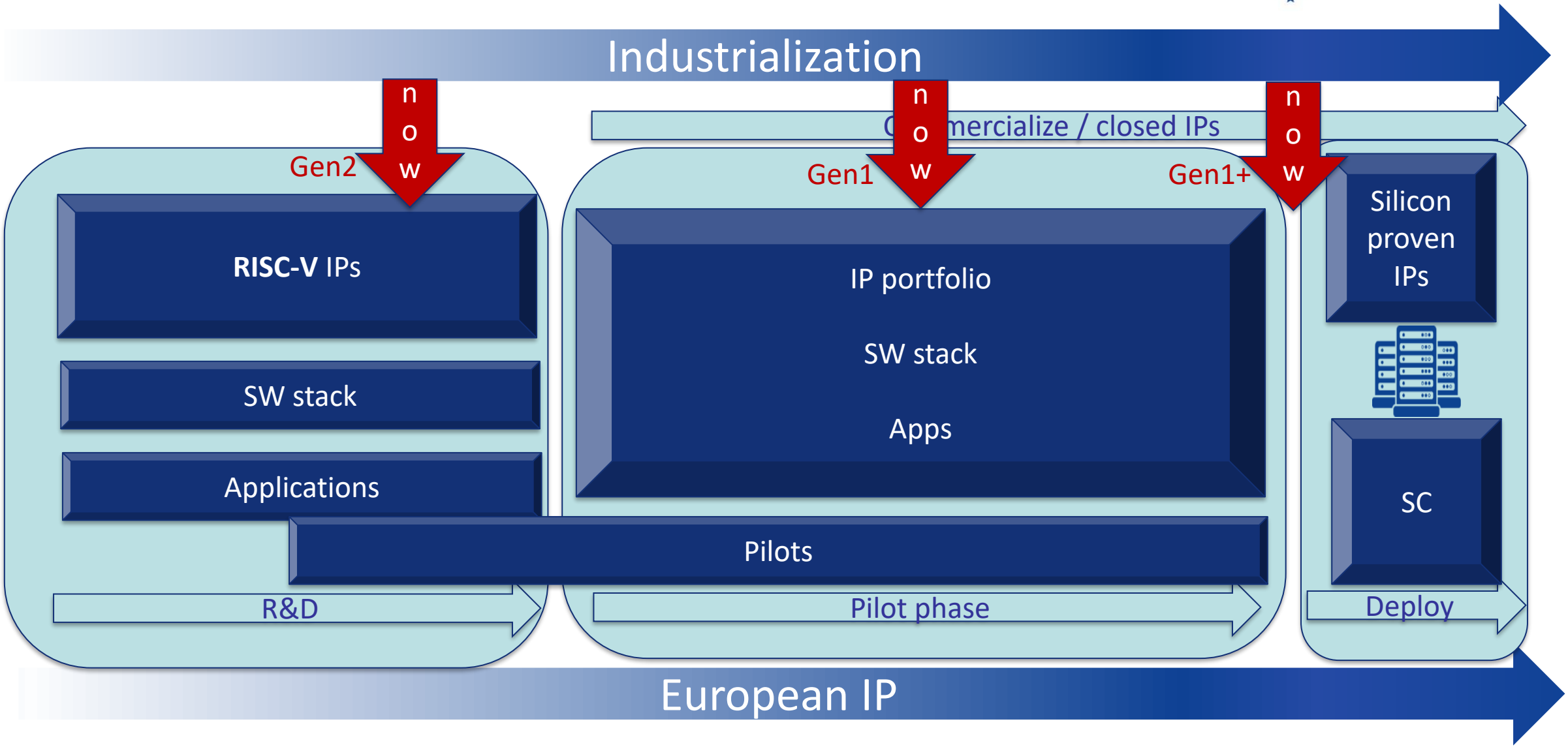


- EPI: European low-power microprocessor technologies
- DARE: Large-scale European initiative for High Performance Computing ecosystem based on RISC-V

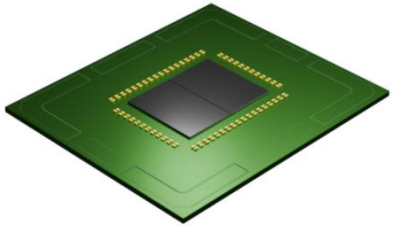
ARM Roadmap


Industrialization
Commercialize / closed IPs
now
ARM IPs
SW stack
Applications
IP portfolio
SW stack
Apps
Silicon proven IPs
SC
Pilots
R&D
Pilot phase
Deploy
European IP

RISC-V Roadmap



ARM Processor development status



RHEA1 – In the fab

- 80 ARM neoverse V1
- HBM, PCIe
- DDR
- 6nm TSMC

RISC-V chips development status

EPI: operational

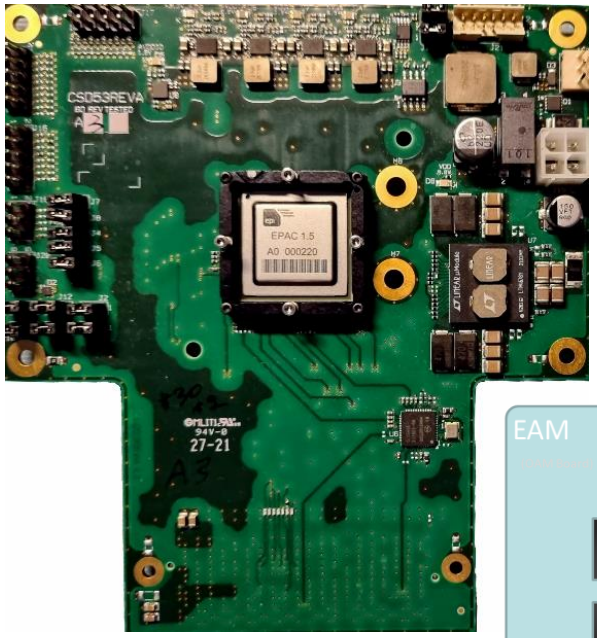
- EPAC 1.5 (2nd gen)
- STX
- SDV

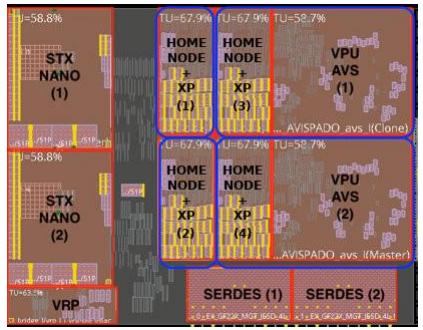
EUPILOT: in the fab

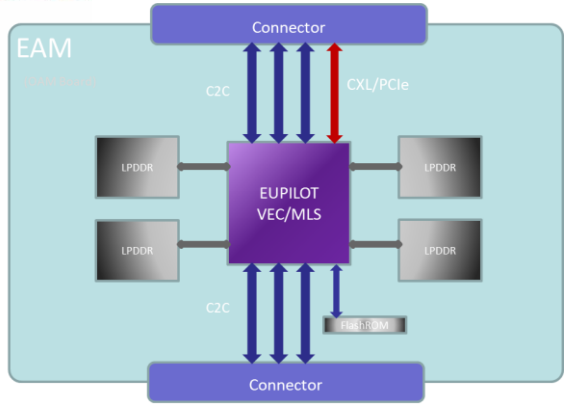
- VEC: Global Foundries 22 nm
- Next GEN:
  - VEC : 59 mm² GF 12nm
  - MLS : 20 mm² TSMC 7nm

eProcessor: bringup complete

- 1 RVOOO core, 1 eAccelerator, 2 L2 slices
- GF 22nm, 10.40 mm²







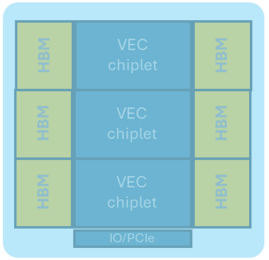
RISC-V chips development status

GPP – RTL design

- High-performance, configurable and customizable OoO RISC-V core
- HW/SW co-design

AIPU – RTL design

- High-performance, energy-efficient AI Inference chiplet
- Complete compiler and software stack

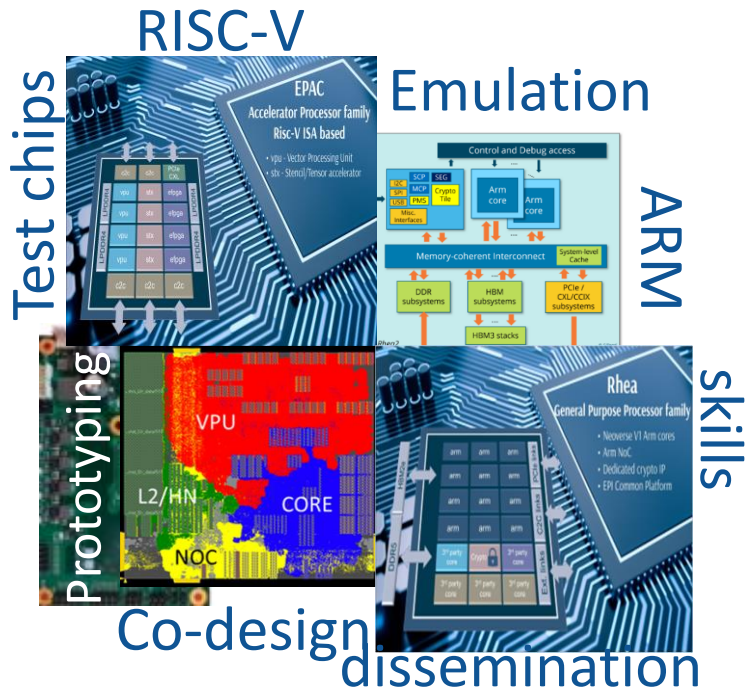


VEC – RTL design

- OOO RISC-V core
- RVV 1.0, multi lane long vector VPU
- matrix extension for AI, HBM
- Software stack

European Processor Initiative at EuroHPC

EPI umbrella and ecosystem



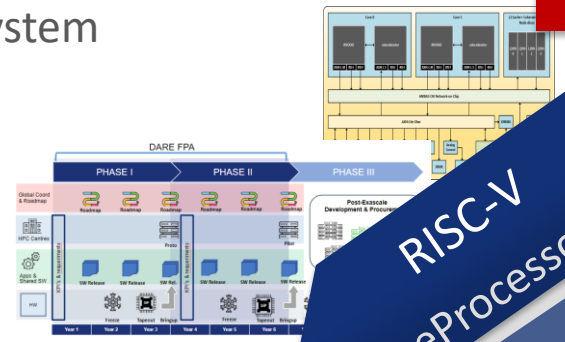
European Processor Initiative at EuroHPC

EuroHPC Joint Undertaking

EPI umbrella and ecosystem

8 M€

240 M€



RISC-V
DARE, eProcessor, ...

ARM
RHEA family

RISC-V

Test chips

Emulation

ARM

EPI

Prototyping

skills

Co-design

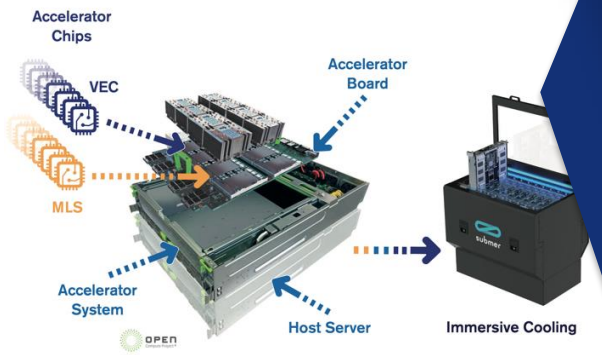
dissemination

EUPILOT

EUPEX

150 M€

40 M€

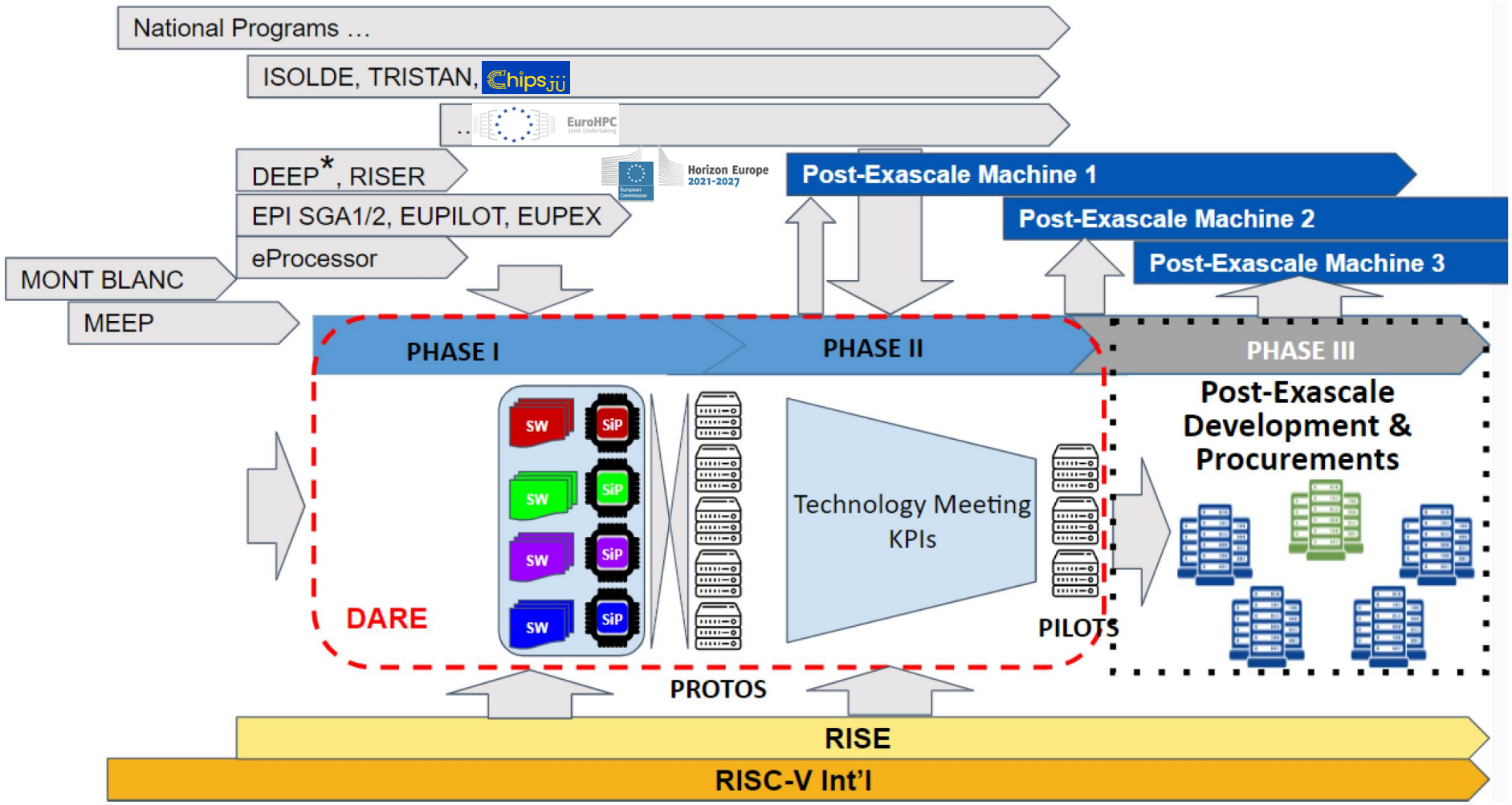


30 M€

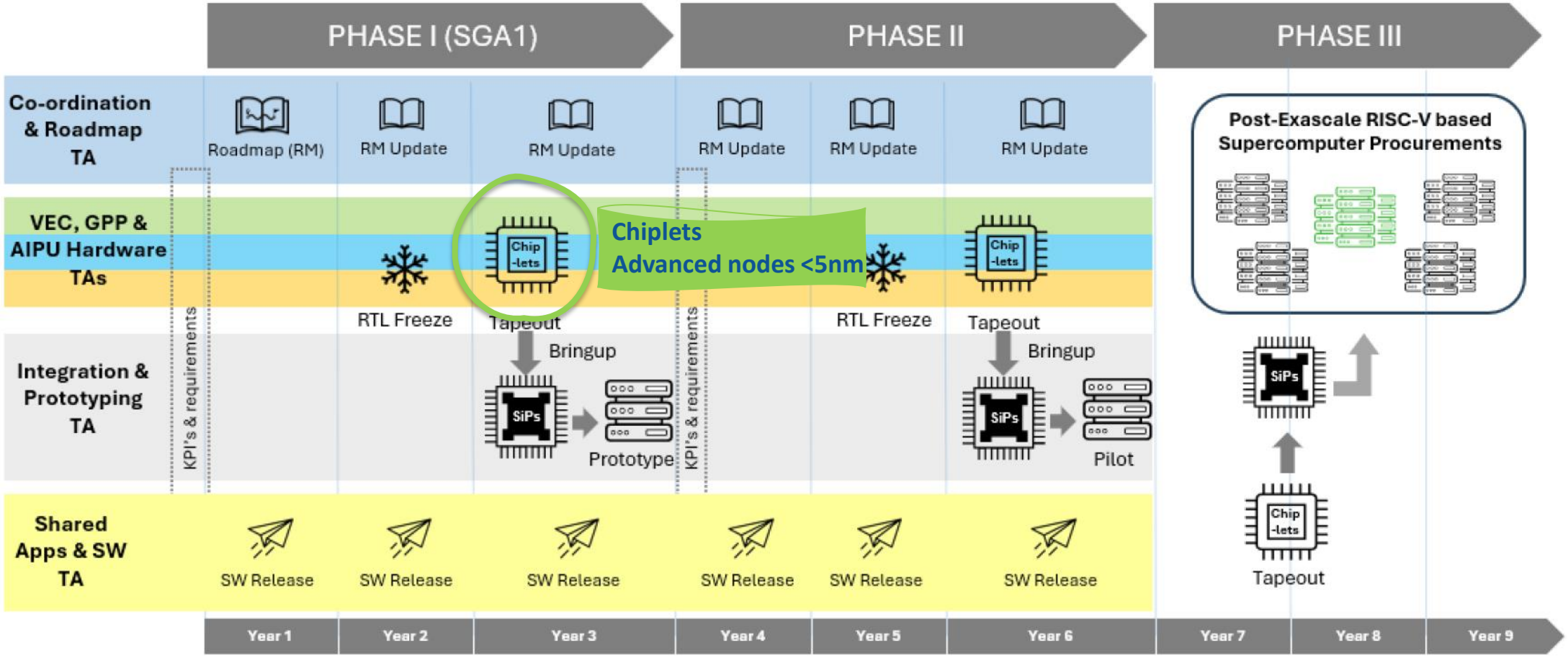
European Processor Initiative at EuroHPC

EPI umbrella and ecosystem

Digital Autonomy with RISC-V in Europe



dare Roadmap



DARE Technical Areas

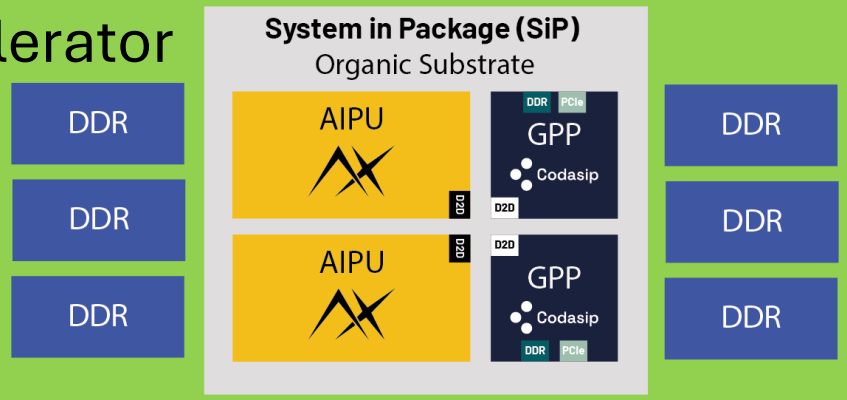
BSC Coordination

(Roadmap, Technical Coordination, PMO, Diss & Inn)

JSC & BSC Shared Software

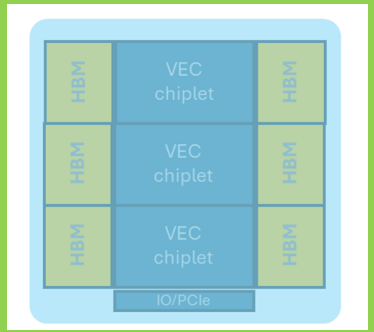
Axelera: AI Inference Accelerator

CODASIP: GPP



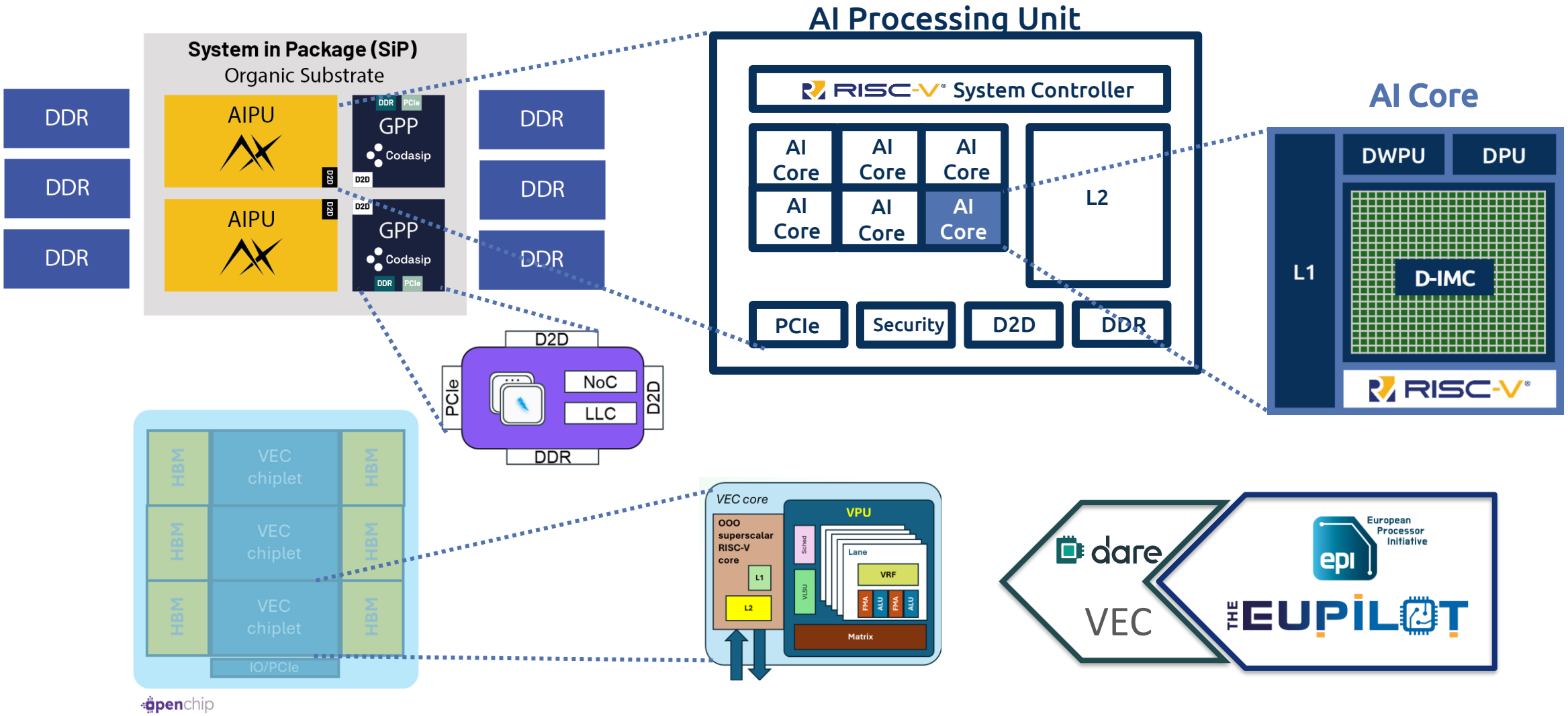
Openchip

Vector Accelerator

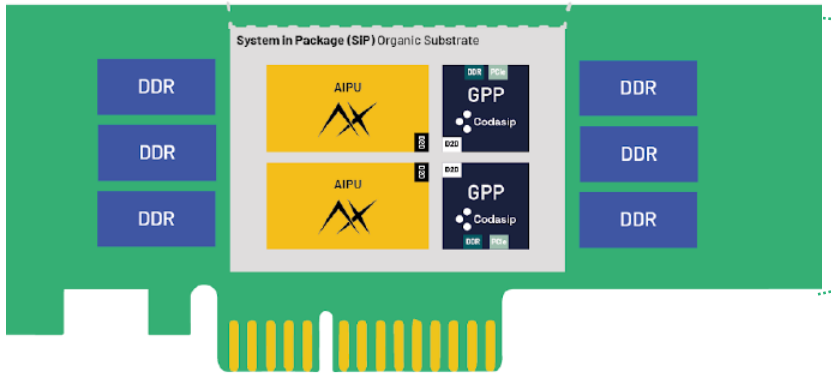


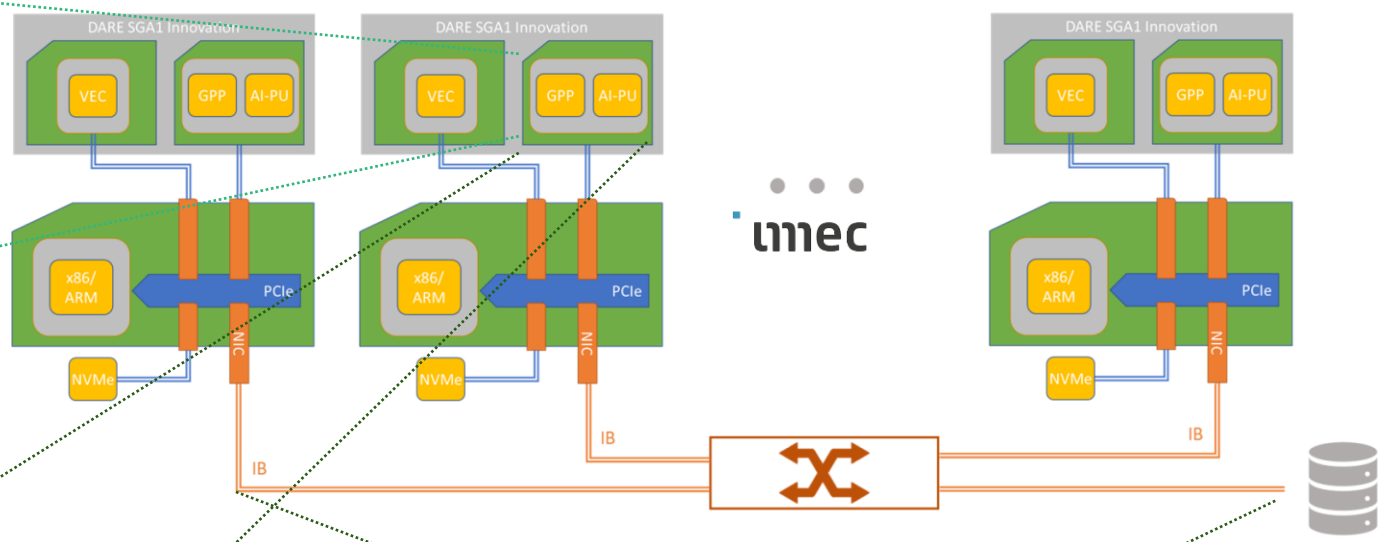
IMEC packaging, testing

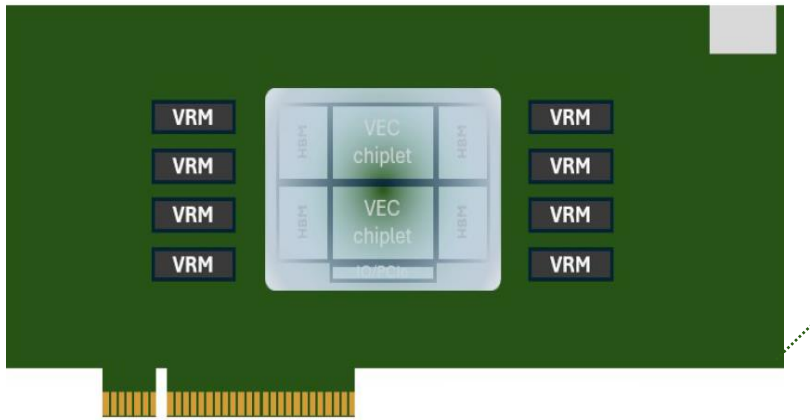
DARE Technical Areas : Chiplets

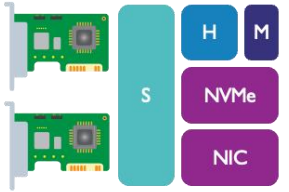


DARE Technical Areas : Integration



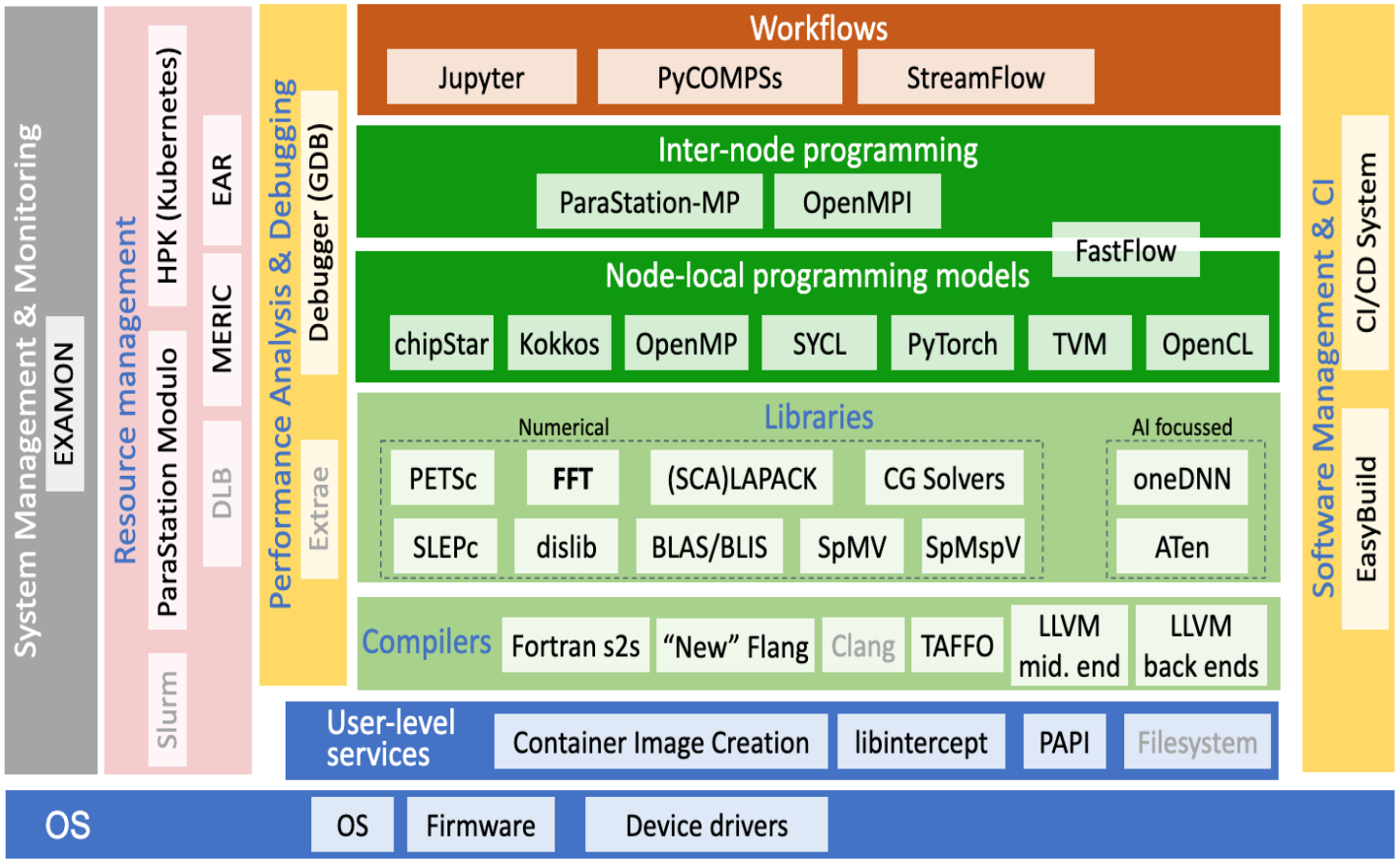






Machine ~ 1000 Nodes	Server ~ 2x-4x Nodes	Node = Host + Devices
Machine = 128x-256x Racks Rack = 8x-16x Servers Network Switches Network Topologies	Multi-Node (2x-4x) Standard Server Config. Network Switches Network Topologies	Host (x86) + Memory PCIe Cards (Devices) Switch (PCIe → CXL) Storage (NVMe)

DARE Technical Areas : SW Stack



- Integrated and optimized **SW stack**
- Based on **existing standards**
  - MPI, OpenMP, Fortran, BLAS, SYCL, PyTorch, …
- Focus on
  - Compilers, especially Fortran
  - Autovectorization and OpenMP
  - Optimized libraries for HPC, AI
  - MPI
- Build on **EU strengths** in HPC & AI
  - Optimize applications and SW stack for DARE chiplets
- HW/SW **co-design**
- Contribute to **Open-Source** SW RISC-V implementations
- Leverage RISC-V **SDVs**

EuroHPC Flagships: Challenges

- Strict timelines: What can be achieved within the limited time-frame?
- RISC-V:
  - » HW/SW co-design and tools not at the same level as competition
  - » EDA, SW stack maturity
  - » Compatible components, not supportive IPs
- Sovereignty
  - » ARM: Not European
  - » Silicon challenges
  - » supply chain, expertise
- Industrial support within Europe:DARE to try or just buy COTS?
- Focus: one ISA or component diversification?

The future

EuroHPC Joint Undertaking

Procurement of AI factories

Procurement of two additional quantum computers to be announced, with quantum chips development opportunities

Delivery of 2nd Exascale supercomputer: Alice Recoque supercomputer (Jules Vernes Consortium) in France, with European IP

Research and Development

- **AI SW stack and applications for exascale and quantum systems**
- **Benchmark framework**

Future Calls - Stay vigilant!

Conclusions

- **ARM & RISC-V for HPC**
  - **Diversity & Inclusiveness**: technology,
  - **Cutting edge** technology: chiplets and advanced nodes
- **SW stack** is crucial
  - One of the most critical parts
- **Consolidated** effort of projects
  - research & industry participation
- Clear, ambitious **vision** & roadmap

The European High Performance Computing Joint Undertaking

LEADING THE WAY IN EUROPEAN SUPERCOMPUTING

October 2025 | **Alexandra Kourfali**

THANK YOU

EuroHPC
Joint Undertaking

For more information, feel free to visit our website and social media:

eurohpc-ju.europa.eu @euroHPC_JU eurohpc-ju @eurohpc-ju